Abstract of the Disclosure

A network processor that has multiple processing

elements, each supporting multiple simultaneous program threads

5   with access to shared resources in an interface. Control logic

in the interface samples the ready state of network ports and

forwards the ready state information to a scheduler-program

thread. The scheduler program thread issues receive request

command that direct the interface to fetch segments of data from

10   a selected one of the network ports into a receive FIFO for

processing by an assigned one of a plurality of receive

processing program threads. For each segment of data that is to

be transferred to the receive FIFO, a control FIFO is loaded with

control information specifying the associated receive FIFO

15   location(s), the selected one of the network ports and the

assigned receive processing program thread. The request is

processed by reading the control information, transferring the

data indicated by the request to the receive FIFO and loading

another control FIFO with control information specifying how the

20   data is to be processed by the assigned receive processing

program thread. The interface signals the assigned receive

processing program thread to process the data.

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